



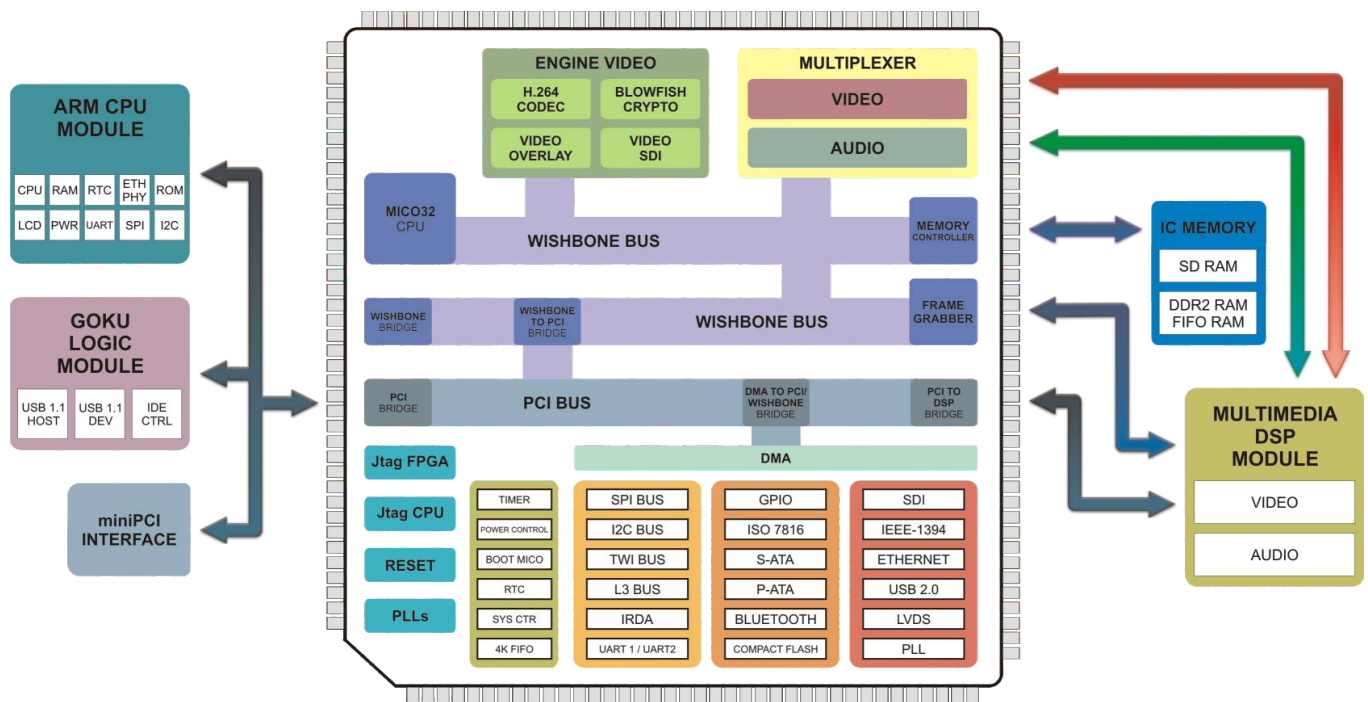
PAIPER

*face*tm
**FPGA & ASIC
CUSTOM ENGINEERING**



PAIPER FACE-VEO I

MULTIMEDIA SPECIALIZED FPGA MULTICORE



Custom FPGA Applications

- **PCI Interface**, 32 Bit/33MHz/3.3V PCI Device core with Irq and DMA feature. This interface (IF) will be used to control configuration register settings. Additionally it can transfer one data stream to or from the main video crossbar unit. The interface will map 4096 bytes in memory address space. No PROM or additional space is provided.
- **DSP-PCI-Workaround** logic block as specified by customer.
- **SPI Device interface** to control configuration register settings. The use of this interface may interfere with simultaneous use of PCI interface. Only one IF may access registers at a time.
- **TWI Controller interface** for control of two-wire compatible devices. The controller will be able act as master. No device feature is provided. The controller will require software support to fully operate. Source code to operate the controller may be provided. Will be controlled via PCI interface only. Will run at up to 400 kHz.
- **SPI-Controller interface** with up to 4 select lines. May send and receive words of up to 32 bit length in one transfer. Will be controlled via PCI interface only. May signal ready status via maskable PCI interrupt if required. Will run with up to 2MHz.
- **UART Multiplexer** to switch the transmit and receive lines of devices to one port. Will be controlled via configuration register set.
- **GPIO Controller** for 32 IO lines, up to 4 of them may generate interrupts via PCI. Will be controlled via configuration register set.
- **Clock controller** for clock distribution. The system will provide 33MHz PCI clock, 27 MHz main video clock and the current audio master clock to the FPGA. These clocks will be used and distributed to all relevant components.
- **Video Overlay Engine (VOE)** will replace marked regions of an SD 656 video stream with a static image. This image will reside in the field memory and may be feed via the PCI bus.
- **Blowfish Crypto Engine** will encrypt and decrypt chunks of data. The engine will use keys stored in the FPGA, these keys are not externally visible. Will run with up to 33MHz.
- **Digital Video Multiplexer** will route several video busses. Signals on these busses run at 75 MHz maximum clock and are single data rate only. It may be necessary to latch the routed video signal to meet signal variance requirements. Endpoints included are PCI and VOE.
- **Digital Audio Multiplexer** will route several audio busses. Signals on these busses run at 25 MHz maximum clock.
- **Configuration Register Set** to set up all muxes and modes of operation. Will be accesible via SPI-Device or PCI-Device interface.